Carbon / high-k Trench Capacitor for the 40nm DRAM Generation


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Outline of Presentation

■ Motivation
■ Properties of Pyrolytic Carbon
■ Integration for the DRAM Capacitor
■ Electrical Results
■ Summary
Carbon as new FEOL Material

- Alternative to metals like TiN and TaN

- Possible Applications:
  - Gate, Contacts, Interconnects,
  - Stress Layer
  - Sacrificial and Mold Material
  - ...

→ Capacitor Electrode in DRAM
Trench Capacitor Road Map

Motivation

Carbon Option

<table>
<thead>
<tr>
<th>Shrink Generation</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIS…Si Insulator Si / MIS…Metal Insulator Si / MIM…Metal Insulator Si</td>
</tr>
</tbody>
</table>

Trench Surface Enhancement

Trench Aspect Ratio

Metal

high-k

110nm 90nm 75nm
NO NO NON
SIS SIS SIS

58nm 48nm
NON / High-k High-k
SIS / MIS MIS / MIM

7.86 µm
Benefits of Carbon

- High Conductivity
- High Temperature Stability
- Integration with NON and high-k viable
- Fills High Aspect Ratios
- Low Cost Pre-Cursors ($C_xH_y$)
- Easily structurable ($O_2$, $H_2$)
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Structural Properties

Graphene Sheets

Desired material is the highly conductive Graphene
Structural Properties

Crystallites with layered structure

High conductivity along the layers
Electrical Resistivity Properties

\[ \rho (\text{m}\Omega \cdot \text{cm}) \]

\begin{align*}
10^{-1} & \quad 10^{0} & \quad 10^{1} \\
10^{-2} & \\
\end{align*}

- TiN
- C
- p-Si

Carbon resistivity can be as low as that of TiN.
Deposition

Nearly 100% step coverage in trench
## Carbon vs. TiN

<table>
<thead>
<tr>
<th>Property</th>
<th>Metal (TiN)</th>
<th>Carbon</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\rho$ ($\mu\Omega$*cm)</td>
<td>50-200</td>
<td>120-2000</td>
</tr>
<tr>
<td>Max. AR shown</td>
<td>1:120</td>
<td>1:430</td>
</tr>
<tr>
<td>Step coverage</td>
<td>&gt;85%</td>
<td>&gt;95%</td>
</tr>
<tr>
<td>Process</td>
<td>pulsed CVD</td>
<td>LPCVD / RTP</td>
</tr>
<tr>
<td>Precursor</td>
<td>TiCl$_4$</td>
<td>$C_xH_y$</td>
</tr>
<tr>
<td>Rate (nm/min)</td>
<td>1-2</td>
<td>0.2 - 120</td>
</tr>
<tr>
<td>Thermal stability</td>
<td>&gt;1200°C</td>
<td>&gt;1200°C</td>
</tr>
</tbody>
</table>
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Etch

- Dry etch by $O_2$ and $H_2$ Plasma

- No attack by wet chemistries
Liner Top Electrode

- Carbon liner as top electrode
- Conductivity gain
- No depletion (Capa gain)

SiO$_2$ insulator
C poly Si
Bulk Top Electrode

- Maximum conductivity gain
- Complexity reduction ➔ no poly fill

Carbon
Void
Surface enhancement (HSG)

SiO₂ insulator
C
poly Si
MIM Application

- C liner top and bottom electrode with high-k
- No depletion for pos. and neg. polarity
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Electrical Resistivity

>Trench capacitor

Cell transistor

Electrical Resistivity

Resistance per Trench (a. u.)

poly-Si, TiN, C

Median
3 Sigma

>50% resistance benefit with Carbon liner application
CET Performance after 1050°C

- CET ~2 w/ planar C/HfSiO/TiN MIM structure
- CET ~3 with C trench top electrode
- NON/C has lower leakage than NON/Si
CET vs. Voltage

- Carbon MIS and MIM application is equivalent to TiN
- Carbon with NON shows capacitance benefit to poly-Si

CET vs. Voltage

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Breakdown Voltage - Reliability after 1050°C

- Carbon on NON has same $V_{BD}$ as w/ poly
- High-k $V_{BD}$ similar with C and TiN
- All options pass reliability
Summary

■ Successfull integration of Carbon as a cost effective enabler of sub 60nm DRAM generations has been demonstrated

■ Carbon is employed as metallic top and bottom electrode in the Deep Trench Capacitor

■ Using standard NON or high-k dielectrics at thermal budgets exceeding 1000°C
Acknowledgements

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